

US-PAT-NO: 5970069

DOCUMENT-IDENTIFIER: US 5970069 A

TITLE: Single chip remote access processor

DATE-ISSUED: October 19, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE
COUNTRY			
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US-CL-CURRENT: 370/402, 370/401, 370/466

ABSTRACT:

A single chip integrated remote access processor circuit has a plurality of communication interface units, including a local area network (LAN) interface unit, a first multi-protocol serial wide area network (SWAN) interface unit, a telephony coder-decoder interface unit and a peripheral component interface (PCI) unit. A data routing control circuit is coupled to the plurality of communication interface units for controlling data transfer between the interface units.

18 Claims, 185 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 83

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Claims Text - CLTX (3):

a multi-channel direct memory access (DMA) controller which is coupled to the plurality of communication interface units and comprises a plurality of channels and a contents addressable memory (CAM), wherein each channel comprises a transmit queue and a receive queue and wherein the CAM comprises a contents compare input coupled to the receive queues so as to receive the destination address of each received data packet and comprises a compare output that identifies which of a plurality of receive linked lists each data packet received by the receive queues is to be appended based on a comparison of the respective destination address;

US-PAT-NO: 5561806

DOCUMENT-IDENTIFIER: US 5561806 A

TITLE: Serial channel adapter

DATE-ISSUED: October 1, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE
COUNTRY			
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US-CL-CURRENT: 709/250

ABSTRACT:

An apparatus for facilitating the transfer of data between computers of different types and architectures is disclosed. The Serial Channel Adapter (SCA) includes four primary functional components: 1) low-end parallel bus interface; 2) data staging buffer; 3) serial interface; and 4) adapter controller, all of which are under microprocessor control and fully programmable to achieve maximum flexibility. Two buses are provided, a Local Data Bus and Local Processor Bus, to minimize processor overhead on the data bus and maximize data throughput.

22 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

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US Patent No. - PN (1):

5561806

Detailed Description Text - DETX (40):

One of the major functions that the SCA provides is the ability to perform Micro Channel master/slave DMA functions that were enabled by the Micro Channel architecture. The MIC chip can perform as a Micro Channel master/slave. It can transfer data in a DMA fashion, as well as communicate over the Micro Channel bus independent of the system processor. What this allows is the removal of the system processor from the communication loop and sets up a direct communication between the SCA via the MIC to other cards at a 80 megabyte rate.

PGPUB-DOCUMENT-NUMBER: 20040022107

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040022107 A1

TITLE: Unidirectional bus architecture for SoC applications

PUBLICATION-DATE: February 5, 2004

INVENTOR-INFORMATION:

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RULE-47			
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US-CL-CURRENT: 365/202

ABSTRACT:

The System-on-Chip apparatus and integration methodology disclosed includes a single semiconductor integrated circuit having one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller (MAC) on a first internal unidirectional bus. The first internal unidirectional bus controls transactions between the processor subsystem(s) the MAC, and the DMA peripheral(s) using a single centralized address decoder and unidirectional, positive-edge clocked address and transaction control signals. The first internal unidirectional bus can support burst operation, variable-speed pipelined memory transactions, and hidden arbitration. The SoC may include a second internal unidirectional bus that controls transactions between the processor subsystem(s) and non-DMA peripherals. The second internal unidirectional bus controls transactions between the processor subsystem(s) and the non-DMA peripheral(s) using unidirectional address and transaction control signals. Peripherals may be synchronous or asynchronous to their respective buses.

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Detail Description Paragraph - DETX (13):

[0060] FIG. 2 illustrates a more complex example with more than one processor. A multi-processor system 200 includes, for example, a digital signal processor (DSP) core 202 connected to a private DSP-bus 204. A memory 206, a cache 208, and a p-bus controller 210 all interface to the DSP-bus 204. A p-bus 212 is common to other processors such as a CPU core 214. A private CPU-bus 216 is connected to a p-bus controller 218, a memory 222, and a cache 224. The p-bus is interfaced to several blocks represented by a pair of blocks 226 and 228. A DMA controller 230 is associated with a refresh controller 232 and several channel controllers 234, 236, and 238, on an m-bus 240. A memory access controller 242 is controlled by a bus arbiter 244 and will allow connections with an external memory bus 246. External memory units are represented by a pair of memories 248 and 250.

Detail Description Paragraph - DETX (68):

[0115] FIG. 23 represents a switched channel memory controller with dual processors in a more complex example where the two processors each have an on-chip dual-port RAM. A switch allows execution by either processor from off-chip flash memory. Data may be transferred to or from a dual-port RAM by a DMA peripheral, or the CPU for processing by the DSP. Or data may be transferred to or from the SDFLAM for CPU processing.

Detail Description Paragraph - DETX (69):

[0116] With a switched channel memory controller, the CPU can execute from flash memory while simultaneously processing data from a DMA peripheral in the SDRAM. The DSP can at the same time process data from the dual-port RAM while another peripheral is transferring data to or from the RAM. With a switched channel memory controller, no changes to any blocks except the memory controller are needed for the processors and DMA peripherals to take best advantage of the available bandwidth.

US-PAT-NO: 6687796

DOCUMENT-IDENTIFIER: US 6687796 B1

TITLE: Multi-channel DMA with request scheduling

DATE-ISSUED: February 3, 2004

INVENTOR-INFORMATION:

NAME COUNTRY	CITY	STATE	ZIP CODE
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US-CL-CURRENT: 711/149, 710/22, 710/38, 710/39

ABSTRACT:

A digital system is provided with a multi-channel DMA controller (400) for transferring data between various resources (401, 402). Each channel includes a source port (460-461), a channel controller (410-412) and a destination port (460, 461). Channel to port buses (CP0-CP2) are representative of parallel buses that are included in the read address bus (RA). Similar parallel buses are provided for a write address bus and a data output bus, not shown. Port to channel buses (PC0-PC1) are representative of parallel buses that are included in data input bus DI. Scheduling circuitry (420, 421) includes request allocator circuitry, interleaver circuitry and multiplexer circuitry and selects one of the channel to port buses to be connected to an associated port controller (460, 461) on each clock cycle for providing an address for a transaction performed on each clock cycle. The schedulers operate in parallel and source/destination channel addresses are transferred in parallel to each scheduler via the parallel channel to port buses. Input/output data words are also transferred in parallel to/from each port. Each port is tailored to provide an access protocol required by its associated resource. The ports may be tailored to provide an access protocol required by a different type of resource. Channel and scheduling circuitry within a sub-portion (400a) of the DMA controller can interact with various versions of tailored ports without being modified.

16 Claims, 26 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 14

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Detailed Description Text - DETX (6):

FIG. 2 is a more detailed block diagram of megacell 100. CPU 200 is a digital signal processor (DSP). CPU 200 accesses memory circuits 220, 222 and 224 via memory interface circuitry 202. CPU 200 accesses external memory via external memory interface (EMIF) 120. CPU 200 access other resources via RHEA bridge 230 to RHEA bus 130. According to an aspect of the present invention, DMA controller 210 is a multi-channel DMA controller with separate channel and port controllers with each port having local scheduling circuitry. DMA 210 can

be programmed to transfer data between various sources and destinations within digital system 10, such as single access RAM 220, dual access RAM 222, external memory 122 via external memory interface 120, and peripheral devices on resource bus (RHEA) 130 via RHEA bridge 230. MCU 110 can also access these resources via host port interface (HPI) 115 which is connected to DMA controller 210. The path between the HPI port and the Memory is a DMA channel.

Detailed Description Text - DETX (14):

This DMA controller meets the need of high rate flow and multi-channel applications such as wireless telephone base stations or cellular handset data traffic.

Detailed Description Paragraph Table - DETL (1):

TABLE 1 Glossary of Terms DMA Direct Memory Access MIF Memory Interface EMIF External Memory Interface HPI Host Port Interface RHEA Resource access bus, for peripheral devices and memory mapped register access SARAM Single Access RAM DARAM Dual Access RAM PDROM Program and Data ROM HOM_M Host Only Mode Memory SAM_M Share Access Mode Memory HOM_R Host Only Mode RHEA SAM_R Share Access Mode RHEA DSP Digital Signal Processor CPU a microprocessor within a megacell on an integrated circuit (IC), such as a DSP. MCU a second processor that interacts with the CPU, may act as a master, or host, processor EHPI Enhanced Host Port Interface. Element the atomic unit of data transferred by the DMA. An element can be a word, 2 words, a burst of 4 words, or a burst of 8 words. Frame set of elements. FIFO first in, first out buffer

Current US Original Classification - CCOR (1):

711/149

US-PAT-NO: 6412029

DOCUMENT-IDENTIFIER: US 6412029 B1

TITLE: Method and apparatus for interfacing between a digital signal processor and a baseband circuit for wireless communication system

DATE-ISSUED: June 25, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE
COUNTRY			
Mecklai; Hussein K.	Whitehall	PA	N/A
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US-CL-CURRENT: 710/22, 711/214, 712/221

ABSTRACT:

A method and apparatus for communicating transmit and receive data between a digital signal processor and the baseband processing circuitry in a digital communications station such as a digital cellular telephone. The invention utilizes a transmit buffer and a receive buffer for smoothing out the flow of data. TRANSMIT BUFFER EMPTY and RECEIVE BUFFER FULL interrupts indicating the need for data to be retrieved from the transmit buffer or sent to the receive buffer, respectively, are serviced by a DMA with translation circuitry rather than the DSP. The DMA with translation circuitry intercepts the interrupts and services them by transferring data directly to or from the DSP's RAM without disturbing the DSP. The translation circuitry also arbitrates between TRANSMIT BUFFER EMPTY and RECEIVE BUFFER FULL interrupts so as to service the RECEIVE BUFFER FULL interrupts first since they have stricter timing requirements.

23 Claims, 4 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

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Abstract Text - ABTX (1):

A method and apparatus for communicating transmit and receive data between a digital signal processor and the baseband processing circuitry in a digital communications station such as a digital cellular telephone. The invention utilizes a transmit buffer and a receive buffer for smoothing out the flow of data. TRANSMIT BUFFER EMPTY and RECEIVE BUFFER FULL interrupts indicating the need for data to be retrieved from the transmit buffer or sent to the receive buffer, respectively, are serviced by a DMA with translation circuitry rather than the DSP. The DMA with translation circuitry intercepts the interrupts and services them by transferring data directly to or from the DSP's RAM without disturbing the DSP. The translation circuitry also arbitrates between TRANSMIT BUFFER EMPTY and RECEIVE BUFFER FULL interrupts so as to service the RECEIVE BUFFER FULL interrupts first since they have stricter timing requirements.

TITLE - TI (1):

Method and apparatus for interfacing between a digital signal processor and

a baseband circuit for wireless communication system

Brief Summary Text - BSTX (4):

In wireless communications systems such as those designed in accordance with the GSM digital cellular telephone standard utilized in Europe, most of Asia (excluding Japan), and other countries, analog data is converted into digital format and modulated on a radio frequency (RF) carrier channel for wireless transmission. At the receiving end, the signal is demodulated back to the baseband and converted back into analog form. Referring to FIG. 1 and using voice data in a digital cellular telephone as an example, in the transmit path, analog voice data from a microphone 12 is converted to digital format by an analog-to-digital converter 14 and encoded by a digital signal processor (DSP) 16. The digital data is commonly processed in a baseband circuit 18 before being forwarded to a modulation circuit 20 for frequency modulating the digital signals onto an RF carrier frequency to be output over an antenna 22.

Detailed Description Text - DETX (4):

In the transmit data path, information is generated and input to the cellular telephone. For instance, information may be voice data input to the telephone via a microphone 12. The voice data is converted to digital format by an analog-to-digital converter 14 and input to the digital signal processor 210. Voice data is merely one type of data that can be transmitted using a cellular telephone. Alternately, digital data can be directly input to the DSP 210 via an interface 46 to which a user may couple a computer to input digital data. The DSP 210 encodes the data in accordance with the GSM protocol and outputs the data to the direct memory access (DMA) 214.

Detailed Description Text - DETX (5):

In accordance with the invention, the DSP need have no knowledge that it is coupled to a DMA. As far as the DSP is concerned, the DMA simply is a peripheral device. The DMA is coupled to a translation block 216. The translation block 216 also is coupled to the transmit buffer 218. The transmit buffer 218 is a buffer for smoothing out data flow in the transmit path. Particularly, it receives the data generated by the DSP 210 and forwards it at the system data rate (e.g., 13/48 MHz) to the baseband processing circuitry 218. As is well known, after baseband processing, the modulation circuitry 20 modulates the digital data onto a radio frequency (RF) carrier and forwards it to the telephone antenna 22 for wireless transmission to a cellular base station.

Current US Cross Reference Classification - CCXR (1):

711/214

US-PAT-NO: 6321299
DOCUMENT-IDENTIFIER: US 6321299 B1
TITLE: Computer circuits, systems, and methods using partial cache cleaning
DATE-ISSUED: November 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE
COUNTRY			
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Jacques			

US-CL-CURRENT: 711/135, 711/129, 711/203, 711/218, 711/219

ABSTRACT:

A method (50) of operating a computing system (10). The computing system comprises a cache memory (12b), and the cache memory has a predetermined number of cache lines. First, the method, for a plurality of write addresses, writes data (64) to the cache memory at a location corresponding to each of the plurality of write addresses. Second, the method cleans (70) a selected number (68) of lines in the cache memory. For each of the selected number of lines, the cleaning step evaluates a dirty indicator corresponding to data in the line and copies data from the line to another memory if the dirty indicator indicates the data in the line is dirty. Lastly, the selected number of lines which are cleaned is less than the predetermined number of cache lines.

29 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

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Drawing Description Text - DRTX (2):

FIG. 1 illustrates a block diagram of a wireless data platform in which the present embodiments may be implemented

Detailed Description Text - DETX (2):

FIG. 1 illustrates a preferred embodiment of a general wireless data platform 10 into which various of the cache embodiments described in this document may be implemented, and which could be used for example in the implementation of a Smartphone or a portable computing device. wireless data platform 10 includes a general purpose (Host) processor 12 having an instruction cache 12a and a data cache 12b, each with a corresponding instruction memory management unit ("MMU") 12c and 12d, and further illustrates buffer circuitry 12e and lastly an operating core 12f, all of which communicate with a system bus SBUS. The SBUS includes data SBUS.sub.d, address SBUS.sub.a, and control SBUS.sub.c conductors. A digital signal processor ("DSP") 14a having its own internal cache (not shown), and a peripheral interface 14b, are

coupled to the SBUS. Although not shown, various peripheral devices may therefore be coupled to peripheral interface 14b, including a digital to analog converter ("DAC") or a network interface. DSP 14a and peripheral interface 14b are coupled to a DMA interface 16 which is further coupled to a DMA controller 18. DMA controller 18 is also coupled to the SBUS as well as to a video or LCD controller 20 which communicates with an LCD or video display 22. DMA controller 18 is coupled via address 24.sub.a, data 24.sub.d, and control 24.sub.c buses to a main memory which in the preferred embodiment is a synchronous dynamic random access memory ("SDRAM") 24. Similarly, DMA controller 18 is coupled via address 26.sub.a, data 26.sub.d, and control 26.sub.c buses to a flash memory 26 (or memories).

Detailed Description Text - DETX (3):

The general operational aspects of wireless data platform 10 are appreciated in connection with the present inventive concepts by noting that it utilizes both a general purpose processor 12 and a DSP 14a. Thus, there are multiple cores sharing a single memory, and it will be appreciated that the inventive methodology described later provides various improvements to system performance for such a multi-core system (which may be the case also for systems other than platform 10). In addition, note that many of the inventive aspects described below also may improve operations in a mono-processor system.

Detailed Description Text - DETX (4):

Turning the focus now to cache aspects of the preferred embodiment, FIG. 2 illustrates by way of example the architecture of data cache 12b of general purpose processor 12 from FIG. 1. Before detailing this structure, it should be understood that various of the present inventive teachings may be implemented in connection with other caches such as instruction cache 12a, either or both of the caches of DSP 14a, or in yet other caches (e.g., unified cache) in platform 10. In addition, various of the inventive teachings described below may be used in conjunction with any processing device which would benefit from a cache memory, including smartphones, PDAs, palmtop computers, notebook computers, desktop computers and so on. Lastly, although various details are presented below with respect to data cache 12b, it also should be noted that many of those details (e.g., set association, array sizes, address and storage lengths) are for illustrative purposes only.

Claims Text - CLTX (83):

wherein the selected number of lines cleaned is less than the predetermined number of cache lines and the computing system comprises a plurality of processors.

Claims Text - CLTX (90):

wherein the selected number of lines cleaned is less than the predetermined number of cache lines and the computing system comprises a wireless data platform system.

Claims Text - CLTX (186):

wherein the selected number of lines cleaned is less than the predetermined number of cache lines and the cache memory is accessible by a plurality of processor cores.